Name: Ahmed Abdeen

ID: 900225815

1)

Ex1:

module SevenSegDec(input [3:0] num, output [6:0] segments);

assign segments [0] = (~num[3] & ~num[2]&~num[1]) | (num[2]&num[1]&num[0]) ;

assign segments [1] = (num[1]&num[0]) | (~num[3]&~num[2]&num[0])| (~num[2]&num[1]);

assign segments [2] = (~num[3]&num[0]) | (num[3]&num[0]) | (num[2]&~num[1]);

assign segments [3] =(~num[3]&~num[2]&~num[1]&num[0]) | (num[2]&num[1]&num[0])| (num[2]& ~num[1]&~num[0]) ;

assign segments [4] = (~num[2]&num[1]&~num[0]);

assign segments [5] = (num[2]&~num[1]&num[0]) | (num[2]&num[1]&~num[0]);

assign segments [6] = (num[2]&~num[1]&~num[0]) | (~num[3]&~num[2]&~num[1]&num[0]);

endmodule

2)

module LabReport5(input[1:0] s, input [1:0]I, output reg F);

always @ (s or I) begin

case(s)

2'b00: F = I [0] & I [1];

2'b01: F = I [0] | I [1];

2'b10: F = I [0] ^ I [1];

2'b11: F = ~I [0];

endcase

end

endmodule

3)

module Lab5report2(input [1:0] I, output reg [6:0] S);

always @ (I) begin

case(I)

2'b00: S = 7'b110001;

2'b01: S = 7'b0111001;

2'b10: S = 7'b1000111;

2'b11: S = 7'b1001000;

endcase

end

endmodule

4)

Test bench for ex2

module Lab5reportQ2Test();

reg [1:0]s;

reg[1:0]I;

wire F;

LabReport5 M1(.s(s),.I(I),.F(F));

initial begin

s[0] = 1'b0;

s[1]= 1'b0;

I[0] = 1'b1;

I[1] = 1'b0;

#100

s[0] = 1'b0;

s[1]= 1'b0;

I[0] = 1'b0;

I[1] = 1'b0;

#100

s[0] = 1'b0;

s[1]= 1'b0;

I[0] = 1'b0;

I[1] = 1'b1;

#100

s[0] = 1'b0;

s[1]= 1'b0;

I[0] = 1'b1;

I[1] = 1'b1;

#100

s[0] = 1'b0;

s[1]= 1'b1;

I[0] = 1'b1;

I[1] = 1'b0;

#100

s[0] = 1'b0;

s[1]= 1'b1;

I[0] = 1'b0;

I[1] = 1'b1;

#100

s[0] = 1'b0;

s[1]= 1'b1;

I[0] = 1'b1;

I[1] = 1'b1;

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s[0] = 1'b0;

s[1]= 1'b1;

I[0] = 1'b0;

I[1] = 1'b0;

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s[0] = 1'b1;

s[1]= 1'b0;

I[0] = 1'b1;

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s[0] = 1'b1;

s[1]= 1'b0;

I[0] = 1'b0;

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s[0] = 1'b1;

s[1]= 1'b1;

I[0] = 1'b1;

I[1] = 1'b0;

#100

s[0] = 1'b1;

s[1]= 1'b1;

I[0] = 1'b0;

I[1] = 1'b1;

#100

s[0] = 1'b1;

s[1]= 1'b1;

I[0] = 1'b1;

I[1] = 1'b1;

#100

s[0] = 1'b1;

s[1]= 1'b1;

I[0] = 1'b0;

I[1] = 1'b0;

end

endmodule

test bench for ex3

module Lab5reportQ3Test();

reg [1:0]I;

wire [6:0]S;

Lab5report2 M1(.I(I),.S(S));

initial begin

I[0] = 1'b0;

I[1] = 1'b0;

#100

I[0] = 1'b0;

I[1] = 1'b1;

#100

I[0] = 1'b1;

I[1] = 1'b0;

#100

I[0] = 1'b1;

I[1] = 1'b1;

end

endmodule